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TITLE OF INVENTION: MULTI-LAYER Pt ELECTRODE FOR DRAM AND FRAM WITH HIGH K DIELECTRIC MATERIALS

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

MULTI-LAYER Pt ELECTRODE FOR DRAM AND FRAM WITH HIGH K DIELECTRIC MATERIALS

TECHNICAL FIELD

The present invention relates generally to the fabrication of integrated circuits (IC's), and more particularly to the fabrication of memory IC's.

BACKGROUND OF THE INVENTION

Semiconductor devices are used in a variety of electronic applications, such as personal computers and cellular phones, for example. One such semiconductor product widely used in electronic systems for storing data is a semiconductor memory, and one common type of semiconductor is a dynamic random access memory (DRAM). A DRAM typically includes millions or billions of individual DRAM cells, with each cell storing one bit of data. A DRAM memory cell typically includes an access field effect transistor (FET) and a storage capacitor. The access FET allows the transfer of data charges to and from the storage capacitor during reading and writing operations. In addition, the data charges on the storage capacitor are periodically refreshed during a refresh operation.

Another memory semiconductor device is called a ferroelectric random access memory (FRAM). An FRAM typically has a similar structure to a DRAM but is comprised of materials such that the storage capacitor does not need to be refreshed continuously as in a DRAM. Common applications for FRAM's include cellular phones and digital cameras, for example.

The semiconductor industry in general is being driven to decrease the size of semiconductor devices located on integrated circuits. Miniaturization is generally needed to accommodate the increasing density of circuits necessary for today's semiconductor products. A

challenge producing memory devices such as DRAM's and FRAM's is maintaining the minimum amount of charge that must be stored in a storage capacitor to obtain reliable operation of the memory device. One way to increase the capacitance density of memory devices is to use higher permittivity capacitance dielectric materials such as barium-strontium titanate $(Ba,Sr)TiO_3$ (BSTO).

Shown in Figure 1 is a cross-sectional view of a prior art DRAM stacked capacitor structure, with a storage capacitor 18 above a bit line contact 16 and connecting to underlying devices through polysilicon plugs 17. The capacitor structure 18 is built upon a substrate 12 which typically comprises polysilicon and may also include underlying semiconductor layers and structures. Word line 14 and bit line 16 provide an address array to enable the programming or charging, or reading of the capacitor 18 during use. Cell plate 28 overlies the high dielectric constant (k) material 26 which may comprise BSTO, for example. Bottom electrode 24 comprises platinum (Pt) overlying a conductive barrier layer 22. Pt is typically used because of its superior work function. The barrier layer 22 comprises a conductive material and is used to separate the electrode 24 from the plug material 20 to prevent electrode-plug interdiffusion and reaction. Barrier layer 22 also protects the plug 17 against oxygen exposure during the deposition of the BSTO dielectric 26, which typically occurs in a high temperature oxygen environment at temperatures in the range of 450 to 700°C. The high dielectric constant material 26 conformally coats the bottom electrode 24, and the counter-electrode forms a plate 28 that is common to an array of a plurality of capacitors 18.

A problem with the stacked capacitor structure 18 using a high dielectric constant material 26 shown in

Figure 1 is that upon deposition of the high dielectric constant material 26, oxygen diffuses through the platinum of electrode 24 to barrier layer 22, forming an oxide layer 30 between bottom electrode 24 and conductive barrier layer 22. Oxide layer 30 comprises an interfacial low dielectric layer between electrode 24 and barrier layer 22 and is typically about 15 nm thick.

The formation of oxide layer 30 is problematic because the bottom electrode is required to be conductive. Oxide 30 typically comprises a non-conductive oxide such as such as $TaSiN_xO_y$, creating an open in the bottom electrode 24, or increasing the resistance of the bottom electrode 24. A similar oxide barrier layer may also form between Pt 24 and plug 17 during BSTO deposition if no barrier layer 22 is used.

What is needed in the art is a memory cell bottom electrode design and method of fabrication thereof that prevents the formation of a non-conductive oxide 30 within the bottom electrode.

In Japanese Patent No. 10-242078 entitled "Multi-Layer Electrode Using Conductive Oxide," issued to Sharp Corporation and published on September 11, 1998, a multi-layer electrode is proposed, in which a conductive barrier layer 122 is formed, and a layer of Iridium (Ir) 132 is deposited over barrier layer 122, as shown in Figure 2. A relatively thick layer of Iridium oxide (IrO_2) 134 is deposited over the Ir layer 132, as shown in Figure 2. Pt electrode material 124 is deposited over the IrO_2 layer 134.

While the Ir layer 132 and IrO_2 layer 134 are conductive and inhibit oxygen diffusion to the poly silicon underneath the barrier liner 122, the structure shown in Figure 2 is disadvantageous because the excessive thicknesses of the Ir layer 132 and IrO_2 layer 134 do not permit the use of the same etchant gas as used

to process the Pt material 124, for example. Therefore, several different etchant gases are required to pattern the electrode, requiring increased labor, time, and an increase in the number and variety of processing chemicals.

SUMMARY OF THE INVENTION

The present invention achieves technical advantages as a multi-layer platinum electrode for use in memory devices having high dielectric constant materials. A multi-layer electrode stack having a thin conductive oxide layer to control the electrode texture prevents oxygen diffusion through the electrode. The thin conductive oxide layer is etchable with the same gases used to etch the conductive electrode materials.

Disclosed is a multi-layer electrode for an integrated circuit, including a conductive barrier layer, a first conductive liner deposited over the conductive barrier layer, a second conductive liner deposited over the first conductive liner, and a conductive layer deposited over the second conductive liner, where the conductive layer and the first conductive liner comprise the same material.

Also disclosed is a multi-layer electrode for an integrated circuit, comprising a conductive barrier layer, a first conductive liner deposited over the conductive barrier layer, a second conductive liner comprising a conductive oxide deposited over the first conductive liner, and a conductive layer deposited over the second conductive liner.

Further disclosed is a method of fabricating an electrode of an integrated circuit, comprising depositing a conductive barrier layer over a substrate, depositing a first conductive liner over the conductive barrier layer, depositing a second conductive liner over the first

conductive liner, and depositing a conductive layer over the second conductive liner, where the conductive layer and the first conductive liner comprise the same material.

Advantages of the invention include prohibiting oxygen diffusion through the multi-layer electrode to the barrier layer interface, preventing the formation of an oxide layer which can cause an open and increase the resistance of the electrode. Material variation is reduced during electrode patterning, for example, the same etchant gas may be used to pattern the conductive layer of the electrode and the first and second conductive liners. The method and structure described herein may be used and applied to a variety of memory integrated circuits, such as DRAM's and FRAM's. The columnar grain growth of Pt is stopped by the insertion of the conductive oxide layer between two Pt layers in accordance with the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The above features of the present invention will be more clearly understood from consideration of the following descriptions in connection with accompanying drawings in which:

Figure 1 illustrates a cross-sectional view of a prior art DRAM stacked capacitor having a non-conductive oxide layer formed between the barrier layer and the bottom electrode;

Figure 2 illustrates a cross-sectional diagram of a prior art multi-layer bottom electrode;

Figures 3-10 show cross-sectional views of a multi-layer electrode for a memory cell in accordance with the preferred embodiment of the present invention at various stages of fabrication;

Figures 11-15 show cross-sectional views of an alternate process flow for the process shown in Figures 6-10;

Figure 16 illustrates a prior art grain structure of a bottom electrode; and

Figure 17 illustrates a cross-sectional view of the grain structure of the electrode of the present invention.

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A description of preferred embodiments of the present invention will be discussed, followed by a comparison of prior art electrode molecular grain structures with the present invention molecular structure, and a discussion of some advantages of the invention. Only one electrode is shown in each figure, although many electrodes and other components of a memory cell are present in the semiconductor devices shown.

Figures 3-14 show two preferred embodiments of the present multi-layer memory electrode invention in various stages of fabrication. Figure 3 shows a cross-sectional view of a semiconductor memory device having a workpiece 202. Workpiece 202 preferably comprises a semiconductor substrate such as silicon. Alternatively, other circuit components may reside within workpiece 202, although the top surface of the workpiece 202 preferably comprises an oxide such as silicon dioxide, for example. In accordance with the present invention, an insulating layer 204 is deposited over workpiece 202. Insulating

layer 204 preferably comprises silicon oxide (SiO_2), and may alternatively comprise other dielectric materials. Insulating layer 204 is patterned and etched to form trenches 205, as shown. Trenches 205 represent areas where conductive vias will be formed in subsequent processing steps.

A layer of conductive material 206 is deposited over the insulating layer 204 and exposed portions of the substrate 202 to fill trench 205, as shown in Figure 4. Conductive layer 206 preferably comprises poly-crystalline silicon (polysilicon), and may comprise other conductive materials suitable to electrically couple the bottom electrode to a word or bit line contact beneath the structure shown (similar to the structure shown in Figure 1).

The wafer is exposed to a chemical-mechanical polish (CMP) to expose insulating layer 204, as shown in Figure 5.

Next, two processes to form the bottom electrode structure will be described. The first process forms a recessed structure, which process flow is shown in Figures 6 - 10, and the second process forms a non-recessed structure, which process flow is shown in Figures 11 - 15.

For the recessed structure process, the conductive material 206 is etched to remove a portion of the polysilicon from the top of the trench 205 and leave a recess, shown in Figure 6. Three liners 222, 240, 242 and a conductive layer 224 are deposited with an in situ deposition, shown in Figure 7. A conductive barrier layer 222 is deposited over insulating layer 204 and polysilicon material 206 in the trench. Conductive barrier layer 222 preferably comprises TaSiN, for example, and may alternatively comprise other conductive materials. Preferably, conductive barrier layer 222

comprises -500 Angstroms of TaSiN, and more preferably comprises 100-300 Angstroms of TaSiN.

A first conductive liner 240 is deposited over conductive barrier layer 222. First conductive liner 240 preferably comprises Pt, and may alternatively comprise other conductive materials such as Ir, Ru, Pd or combinations thereof, for example. First conductive liner 240 preferably comprises the same material as the material to be subsequently deposited for conductive layer 224. Preferably, the first conductive liner 240 comprises 100-500 Angstroms of Pt, and more preferably comprises 200 Angstroms of Pt.

A second conductive liner 242 is deposited over the first conductive liner 240. Second conductive liner 242 preferably comprises a conductive oxide such as Iridium oxide (IrO_2), or alternatively, Ruthenium oxide (RuO_2), for example. Preferably, the second conductive liner 242 comprises 20-500 Angstroms of conductive oxide, and more preferably comprises 20-50 Angstroms of conductive oxide.

A layer of conductive material 224 is deposited over the second conductive liner 242. Conductive layer 224 preferably comprises Pt, and may alternatively comprise other conductive materials such as Ir, Ru, Pd or combinations thereof, for example. Preferably, conductive material 224 comprises 1500-3500 Angstroms of Pt, and more preferably comprises 2200 Angstroms of Pt.

The wafer is exposed to a CMP process to expose insulating layer 204 around the multi-layer electrode, as shown in Figure 8. Because the second conductive liner 242 is thin, the conductive layer 224 can be deposited filling into the recess. The interface between the conductive layer 224 and the second conductive liner 242 will not be exposed during the CMP. This will prevent the surface of second conductive liner 242 from the

contamination and therefore increase the adhesion of the conductive layer 224 on the second conductive liner 242.

Conductive layer 244 is deposited, as shown in Figure 9. Preferably, conductive layer 244 comprises Pt and alternatively may comprise other conductive materials such as Ir, Ru, Pd or combinations thereof, for example. Layer 244 and 224 preferably comprise the same material and are essentially homogenous, and thus, they are shown as one layer 244 in subsequent figures.

The conductive material 244 is patterned and etched to form a conductive region 244, as shown in Figure 10.

In a second embodiment, which comprises a process for fabricating a non-recessed bottom electrode structure, four conductive layers, 322, 340, 342, and 344 are deposited on planarized polysilicon 206 and silicon oxide 204, shown in Figure 11. A conductive barrier layer 222 is deposited over planarized conductive material 206 and insulating layer 204. Conductive barrier layer 322 preferably comprises TaSiN, for example, and may alternatively comprise other conductive materials. Preferably, conductive barrier layer 322 comprises 15-500 Angstroms of TaSiN, and more preferably comprises 100-300 Angstroms of TaSiN.

A first conductive liner 340 is deposited over conductive barrier layer 322. First conductive liner 340 preferably comprises Pt, and may alternatively comprise other conductive materials such as Ir, Ru, Pd or combinations thereof, for example. First conductive liner 340 preferably comprises the same material as the material to be subsequently deposited for conductive layer 324. Preferably, the first conductive liner 340 comprises 100-500 Angstroms of Pt, and more preferably comprises 200 Angstroms of Pt.

A second conductive liner 342 is deposited over the first conductive liner 340. Second conductive liner 342

preferably comprises a conductive oxide such as IrO_2, or alternatively, RuO_2, for example. Preferably, the second conductive liner 342 comprises 20-500 Angstroms of conductive oxide, and more preferably comprises 20-50 Angstroms of conductive oxide.

A layer of conductive material 324 is deposited over the second conductive liner 342. Conductive layer 324 preferably comprises Pt, and may alternatively comprise other conductive materials such as Ir, Ru, Pd or combinations thereof, for example. Preferably, conductive material 324 comprises 1500-3500 Angstroms of Pt, and more preferably comprises 2200 Angstroms of Pt.

The four conductive four conductive layers, 322, 340, 342, and 344 are patterned, for example, by RIE, as shown in Figure 12. Because the second conductive liner 342 is thin, the same etchant gas may be used to etch second conductive layer 342 as used to etch conductive materials 344 and 340.

An insulator layer 348 comprising a dielectric such as SiO_2, is deposited on the patterned conductive layers 322, 340, 342, and 344, as shown in Figure 13. The wafer is planarized, for example, by CMP, shown in Figure 14 and the insulator layer 348 is etched back to a height such that insulator layer 348 will cover the interface of conductive layer 344 and second conductive layer 342, as shown in Figure 15.

Barrier layer 222/322, first conductive liner 240/340, second conductive layer liner 242/340, and conductive region 244/344 comprise a multi-layer electrode 246/346 stack in accordance with the present invention. The thin second conductive stack liner 242/342 controls the electrode conductive layer 244/344 texture, preventing oxygen diffusion through to the barrier layer 222/322.

The differences in the grain structure on a molecular level between the prior art and the present invention will next be described. Figure 16 illustrates a cross-sectional view of a prior art Pt electrode 24 overlying a barrier layer 22. When Pt 24 is deposited using a physical vapor deposition (PVD) as is commonly done in the industry, the Pt has a columnar grain structure, as shown. Columns 38 permit diffusion of oxygen through the grain boundary of Pt 24 to barrier layer 22, which can form an oxide layer and create an open or increase the resistance of the electrode.

Figure 17 shows the molecular grain structure of the present invention having a conductive oxide layer 242 sandwiched between two Pt layers 244 and 240. The columns 238 of the top Pt layer 244 do not coincide with the columns 239 of the lower Pt 240 layer, reducing oxygen diffusion from the top surface to the barrier layer 222. The disconnected grain structure provided by the thin layer of conductive oxide 242 prevents the formation of a non-conductive oxide between the conductive layer 244 and barrier layer 222.

The present multi-layer electrode invention provides several advantages over prior art electrodes for memory semiconductors. The multi-layer electrode 246/346 of the present invention prohibits oxygen diffusion through the electrode to the barrier layer 222/322 interface, preventing the formation of an oxide layer which can cause opens in and increase the resistance of the electrode 246/346. Material variation is reduced during the electrode patterning, resulting in the same etchant gas being able to be used to pattern the Pt electrode conductive layer 244/344 and the first and second conductive liners 240/340 and 242/342. The method and structure described herein may be used and applied to a variety of structures, such as DRAM's, FRAM's, and other

integrated circuit applications where oxygen diffusion is undesired, for example. The columnar grain growth of Pt is stopped by the insertion of the thin conductive oxide layer 242/342 between the two Pt layers 222/342 and 244/344 in accordance with the present invention.

While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications in combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. For example, while the multi-layer electrode invention is described herein with reference to a DRAM, it also has useful application in FRAM and other semiconductor devices. In addition, the order of process steps may be rearranged by one of ordinary skill in the art, yet still be within the scope of the present invention. It is therefore intended that the appended claims encompass any such modifications or embodiments. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.